reference numeral 50 appears to look like a "5C". Support for this correction can be found in the specification at page 13, lines 8-9.

Figures 4, 5, 6, 7, 8, and 9 have been amended to correct a typographical error or omission related to the gate layer, that carries the numerical suffix "22". Support for this correction can be found in the specification at each section that covers the respective Figures. The specification that discusses Figure 9 has an omission in which it erroneously refers to the gate layer as "gate layer 22". However, from the disclosure scheme apparent in the specification, this reference numeral and the supporting text is correctly "gate layer 922".

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 16, 17, and 19-21. The specific amendments to individual claims are detailed in the following marked up set of claims.

16. (Amended) A method of forming a device comprising:

patterning a first oxide layer having a first width upon a substrate;

forming a first nitride layer upon the first oxide layer and the substrate, wherein the first nitride layer has a first thickness that is less than the first width;

forming a first nitride spacer mask from the first nitride layer, wherein the first nitride spacer mask has a width about equal to the first nitride layer thickness;

forming a[n] second oxide layer upon the first nitride spacer mask, wherein the second oxide layer has a second thickness that is less than the width of the first nitride spacer mask;

forming a first oxide spacer mask from the second oxide layer, wherein the first oxide spacer mask has a width about equal to the second [first] oxide layer thickness;

forming a second nitride layer upon the first oxide spacer mask, wherein the second

nitride layer has a thickness that is less than the width of the first oxide spacer mask;

forming a second nitride spacer mask from the second nitride layer;

removing the first oxide spacer mask;

performing an etch over the second nitride spacer mask to form at least one semiconductor channel having a channel width and a length, wherein the mean free electron path therein is larger than the channel width;

forming a dielectric layer upon the channel length; and

forming a gate layer over the channel.

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17. (Amended) The method according to claim 16, wherein the first oxide has a [width of X and a] pitch of about three times the first width [3X].

19. (Amended) The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels, wherein each of the plurality of semiconductive channels has a width of about one-tenth the first width [X];

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

20. (Amended) The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth the first width [X];

removing the patterned second nitride spacer mask;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

21. (Amended) The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth the first width [X];

forming an oxide upon the SOI topology;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic width from about 2 times the first width [X] to about 10 times the first width [X].

22. (Amended) A method of forming a device comprising:

patterning a first oxide upon a substrate, wherein the first oxide has a characteristic width of X and a characteristic pitch selected from about 3X and about 3.2X;

forming a first nitride layer upon the first oxide, wherein the first nitride layer has a characteristic thickness of about one half X;

performing a spacer etch upon the first nitride layer and removing the first oxide to form a patterned first nitride spacer mask;

forming an oxide layer upon the patterned first nitride spacer mask, wherein the oxide layer has a characteristic thickness of about one fourth X;

performing a spacer etch upon the oxide layer and removing the patterned first nitride spacer mask to form a patterned first oxide spacer mask;

forming a second nitride layer upon the patterned first oxide spacer mask, wherein the second nitride layer has a characteristic thickness of about one-tenth X; and

performing a spacer etch upon the second nitride layer and removing the first oxide spacer mask to form a patterned second nitride spacer mask.